Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

14-19. (Withdrawn)

20. (Currently Amended): An integrated circuit, comprising:

a logic inverter comprising:

an n-channel field effect transistor;

a p-channel field effect transistor;

a gate, formed in a layer of polysilicon; and

a connection between a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor formed in said same layer of polysilicon, wherein the polysilicon comprising said gate is coplanar with the polysilicon comprising said connection between said drain of the p-channel field effect transistor and said drain of the n-channel field effect transistor.

21. (Cancelled):

22. (Previously Presented): The integrated circuit as described in claim 20, further comprising:

a first layer of metallization; and

a second layer of metallization, wherein the second layer of metallization comprises substantially no local interconnect.

23. (Previously Presented): The integrated circuit as described in claim 22, wherein said second layer of metallization comprises no local interconnect.

24. (Previously Presented): The integrated circuit as described in claim 20, further comprising:

a plurality of MACROs;

a fist first layer of metallization; and

a second layer of metallization interconnecting said plurality of MACROs.

25. (Cancelled)

26. (Previously Presented): The integrated circuit as described in claim 24, further comprising, no local interconnect within said second layer of metallization in at least one of said MACROs.

27. (Previously Presented): The integrated circuit as described in claim 24, further comprising, no local interconnect within said second layer of metallization in a plurality of said MACROs.

28. (Previously Presented): The integrated circuit as described in claim 24, further comprising, no local interconnect within said second layer of metallization in all of said plurality of MACROs.

29. (Previously Presented): The integrated circuit as described in claim 24, wherein at least one of said MACROs is comprised by a standard cell array of the integrated circuit.

30. (Previously Presented): The integrated circuit as described in claim 29, wherein said standard cell array comprises a row pitch and at least one MACRO has a row pitch equivalent to the row pitch of said standard cell array.